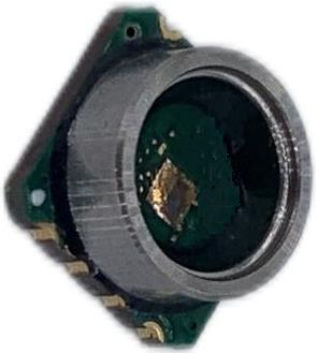


Data Sheet	PSD0603130

General Description

The PSD0603130 is a high-resolution, 4.35psi (30kPa) to 29.02psi (200kPa) pressure sensor in a compact 8-pin LGA package. It features an anti-magnetic stainless-steel enclosure and SPI and I2C interfaces. The PSD0603130 combines high-linearity pressure sensor with an ultra-low-power 24-bit delta-sigma analog-to-digital converter (ΔΣADC). The pressure sensor is factory calibrated. The calibration coefficients are stored internally and used by the ΔΣADC as it processes the sensor's analog output. The PSD0603130 also includes a temperature sensor with a nominal resolution of 0.003°C.

The SPI and I2C interface maximize compatibility with the communication interfaces on a wide range of popular micro-controllers.

Features

- Pressure range: 4.35psi to 29.02psi
- Temperature resolution: 0.003°k/LSB
- 24-bit DSADC
- SPI or I^2C serial interface
- 3.3V_{DC} nominal power supply voltage

Applications

- Barometers
- Mobile altimeters
- Indoor navigation systems
- Industrial pressure and temperature sensing systems
- Pressure and temperature logging systems
- Adventure and sports watches, gas meters
- Weather stations, and oil contact systems.

Electrical Characteristics

Absolute Maximum Ratings (T_A = 25°C, unless otherwise specified.)

Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{DD}		-0.3		5.5	Volts
IO Pin		-0.3		V_{DD}+0.3	Volts
Burst Pressure				289.85	psi
ESD Class	Human Body Model	-2000		2000	Volts
Storage Temperature		-40		125	°C

Performance Characteristics (V_{DD} = 3.3±0.3V, T_A = 25°C, unless otherwise specified.)

Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{DD}		1.8		5.0	Volts
I_{DD}	PGA on; Gain > 4 Sleep Mode		1.8 100	2.8 200	mA nA
ADC Resolution			24		Bits
Operating Temperature		-40		125	°C
Storage Temperature		-40		125	°C
Pressure Characteristics					
Pressure Range		4.35		29.02	psi
Accuracy[1]	-40°C ≤ T_A ≤ -25°C 65°C ≤ T_A ≤ 85°C	-0.058		0.058	psi
	-25°C ≤ T_A ≤ 65°C	-0.029		0.029	
Conversion Time	Cyclic periodic pattern	2.5			ms
Overload Pressure				87.08	psi
Pressure Compensation Temperature Range		-40		85	°C
Pressure Temperature Drift Coefficient			0.00007		psi/°C
Pressure Compensation Temperature Range		-40		125	°C
Temperature Characteristics					
Temperature Resolution			0.003		°C/LSB
Temperature Accuracy	-40°C ≤ T_A ≤ 50°C	-0.5		0.5	
Temperature Compensation Temperature Range		-40		125	°C

Note 1: 11.60psi ≤ P_A ≤ 18.85psi

I2C Interface Characteristics (T_A = 25°C, unless otherwise specified.)

Symbol	Parameters	Conditions	Minimum	Typical	Maximum	Unit
f_{SCL}	Serial Bus Frequency				400	kHz
t_{LOW}	Clock-Low Time		1.3			µs
t_{BHIGH}	Clock-High Time		0.6			µs
t_{SUDATB}	SDA Setup Time		0.1			µs
t_{HDOATB}	SDA Hold Time					µs
t_{SUSTAB}	SDA Valid After Rising CLK Edge Setup Time		0.6			µs
t_{HDSTA}	Delay Between SDA Falling Edge and SCL Falling Edge		0.6			µs
t_{SUSTO}	Delay Between SCL Rising Edge and SDA Rising Edge		0.6			µs
t_{BUF}	Bus Free Time Between Stop and Start Conditions		1.3			µs

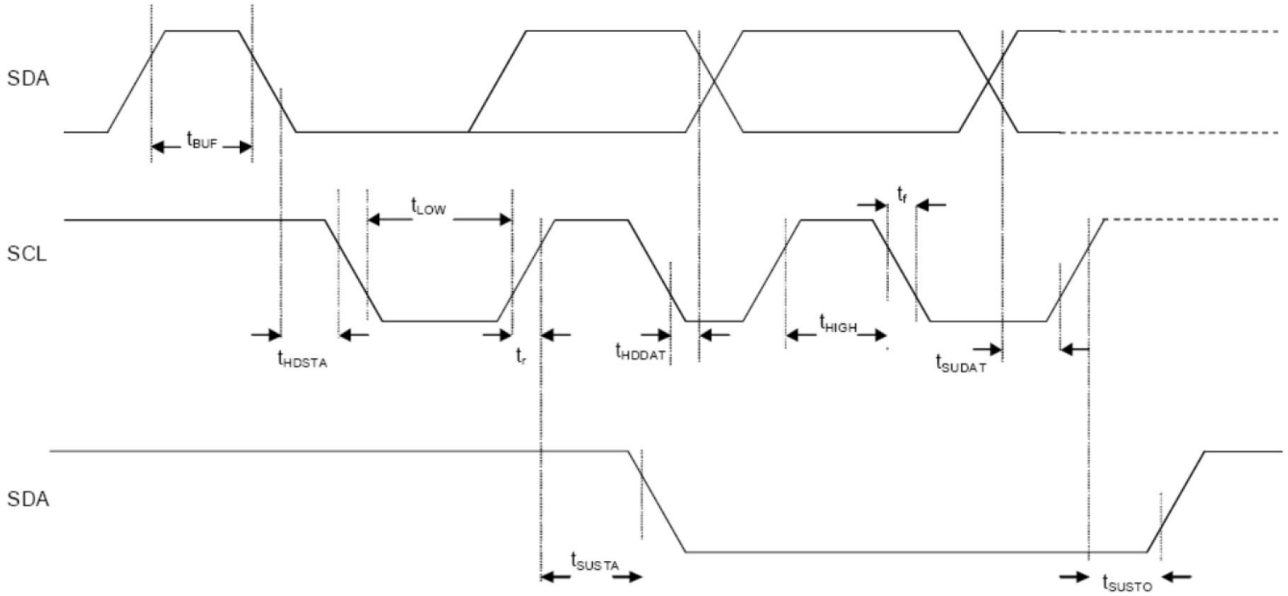


Figure 1. I2C Timing Diagram

SPI Interface Characteristics (T_A = 25°C, unless otherwise specified.)

Symbol	Parameters	Conditions	Minimum	Typical	Maximum	Unit
f_{SCLK}	Serial Bus Frequency	$C_{SD\_LOAD} \leq 25pF$			10	MHz
T_{SCKL}	Clock-Low Time		20			ns
T_{SCKH}	Clock-High Time		20			ns
t_{SDI_setup}	SDA Setup Time		20			ns
T_{SDI_hold}	SDA Hold Time		20			ns
T_{SDO_OD}	SDO Valid After Falling CLK Edge Setup Time	C_{SD_LOAD} = 25pF			30	ns
		C_{SD_LOAD} = 250pF			40	
T_{CSB_setup}	Chip Select Setup Time		20			ns
t_{CSB_hold}	Chip Select Hold Time		40			ns

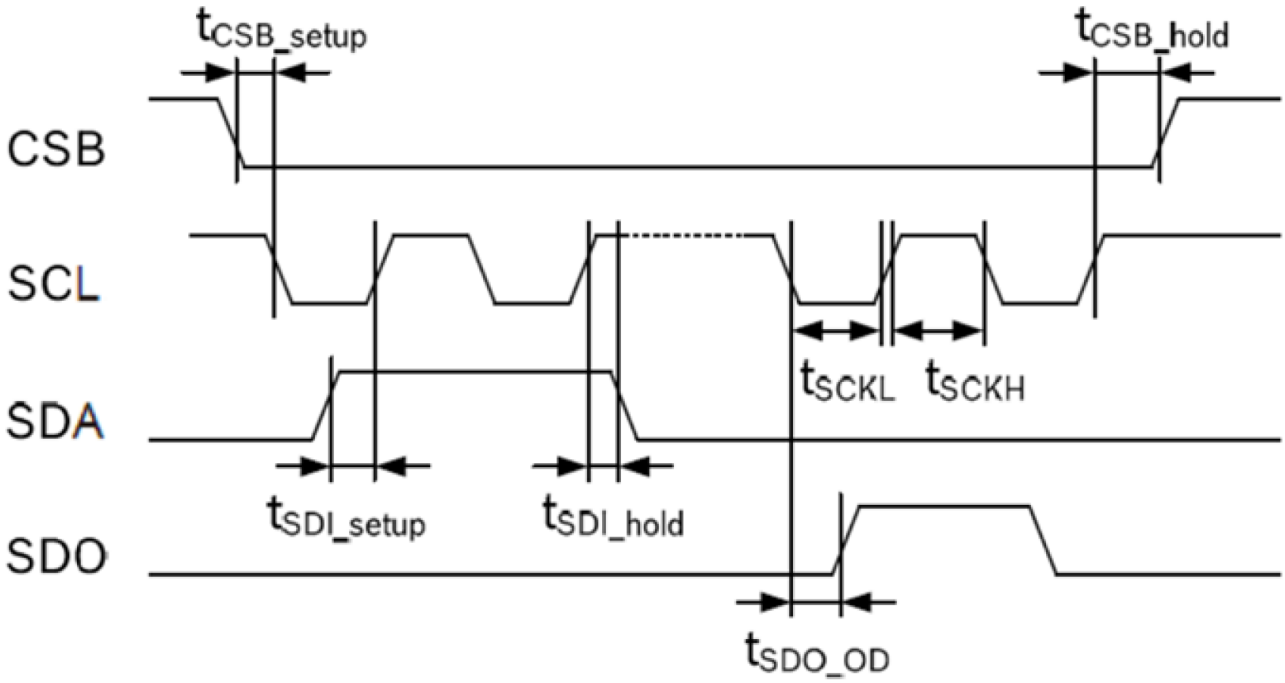
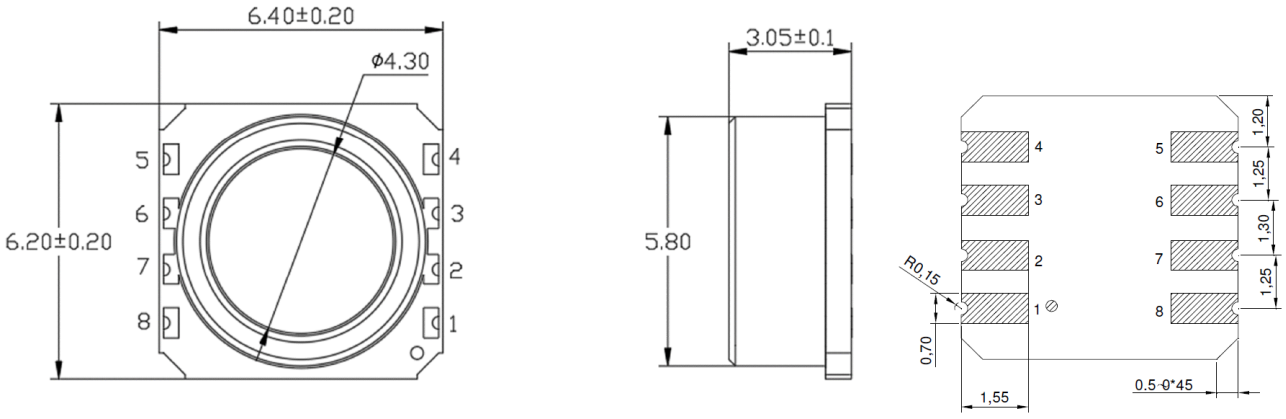


Figure 2. SPI Timing Diagram

Dimensions and Pin Definitions



Pin	Symbol	Description
1	SCL	I²C and SPI serial interface clock input
2	GND	Ground
3	CSB	I²C and SPI interface select, or SPI enable
4	NC	No Connect
5	VDD	Power supply voltage input
6	INT	Interrupt signal - Occurs at the end of a measurement
7	SDA	I²C interface – Data input and output SPI interface – Data input
8	SDO	SPI interface – Data output I²C address end Interrupt signal output

Applications Information

Functional Description

The PSD0603130 uses a MEMS piezoresistive absolute pressure sensor as a pressure detecting element. The digital output is a serial data bit stream, containing data that is proportional to the local ambient atmospheric pressure. The pressure sensor's analog output is amplified by a programmable amplifier (PGA) whose gain is adjustable from 4 to 64. This is followed by a buffer that is designed to drive the DSADC's input capacitance with the necessary current and slew rate to ensure accurate analog to digital conversion. The 24-bit delta-sigma analog to digital converter (DSADC) performs the conversion from the sensor's analog signal to a corresponding digital value and simultaneously applies temperature and linearity compensation. The PSD0603130's block diagram is shown in Figure 3.

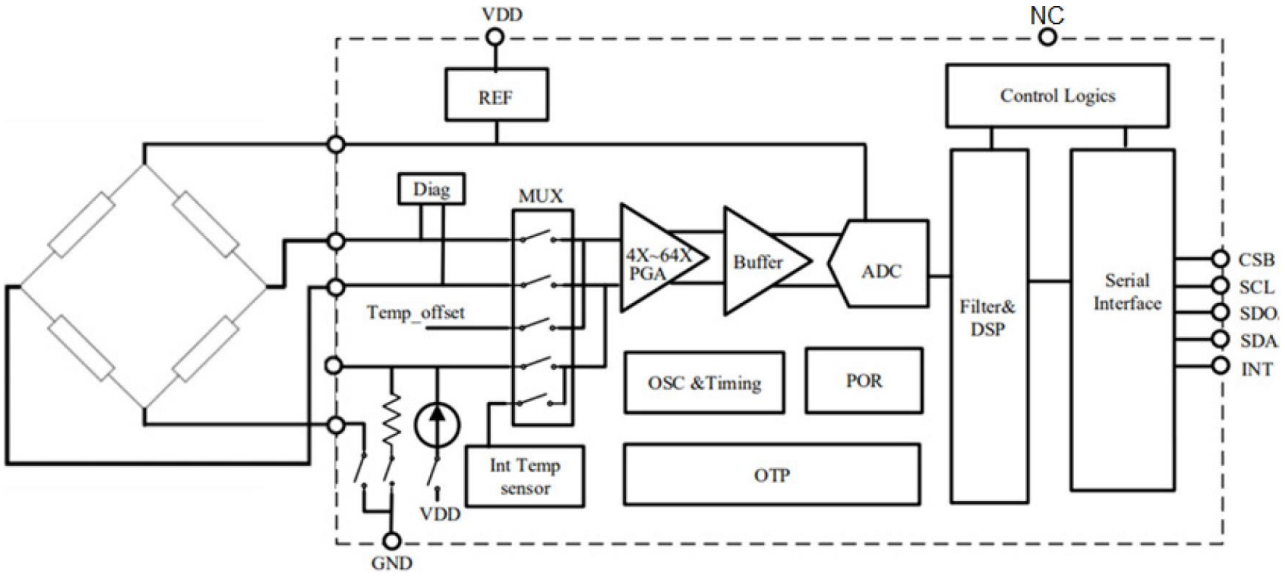


Figure 3. PSD0603130 block diagram.

Serial Communication

The PSD0603130 features both I²C and SPI serial communication interfaces and protocols. Applying a logic high to the SCB pin select I²C. When using an SPI interface, SCB is a chip-select generated by the host processor.

I²C

The PSD0603130's I2C bus uses the SCL and SDA signal pins. Apply V_{DD} through a pull-up resistor (4.7kΩ, nominal) as shown in Figure 4. This ensures that the pins are held at logic high when communication is suspended.

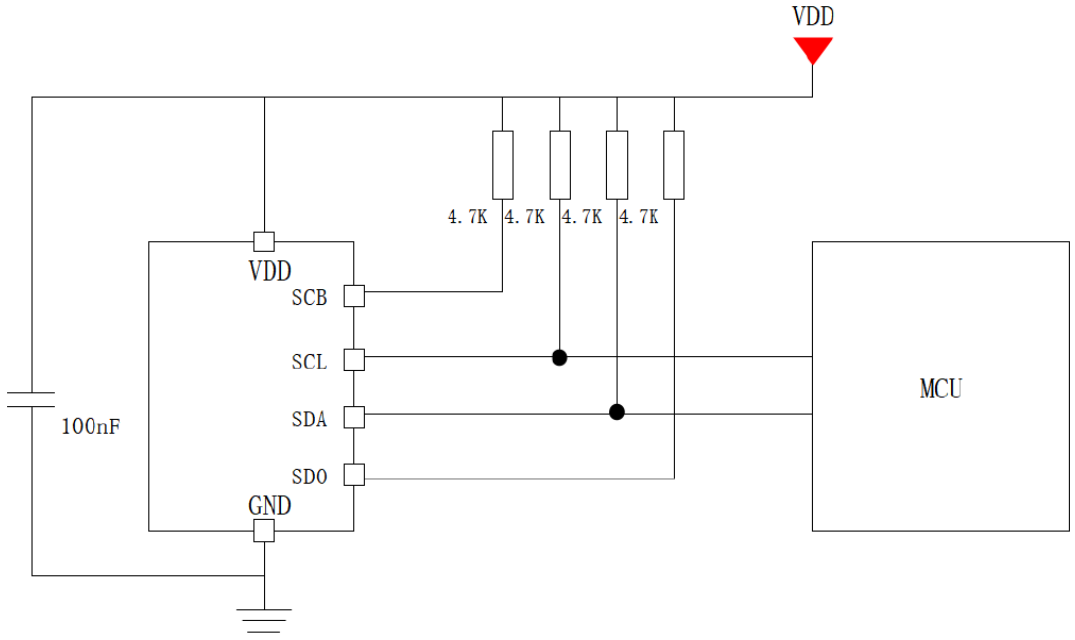


Figure 4. I²C typical application block diagram.

I²C Address

The PSD0603130 offers I²C address flexibility. When SDO is floating, it can be set to the default of 0x6D (7-bits) or 0x8D (8-bits). When SDO is pulled to V_{DD} through a nominal 4.7kΩ resistor, the 7-bit address is 0x6C, whereas the 8-bit address is 0xD8.

A7	A6	A5	A4	A3	A2	A1	W/R
1	1	0	1	1	0	SDO/ADDR	0/1

Table 1. I2C address map.

The I2C master device sends an MSB-first 8-bit address (the eighth bit designates a write to (W/R bit = 0) or read from (W/R bit = 1)), the Slave device.

I2C Communication Protocol

The I²C communication protocol has a start and a stop condition. The start condition occurs when the logic states on SDA and SCL are shown in Figure 5.

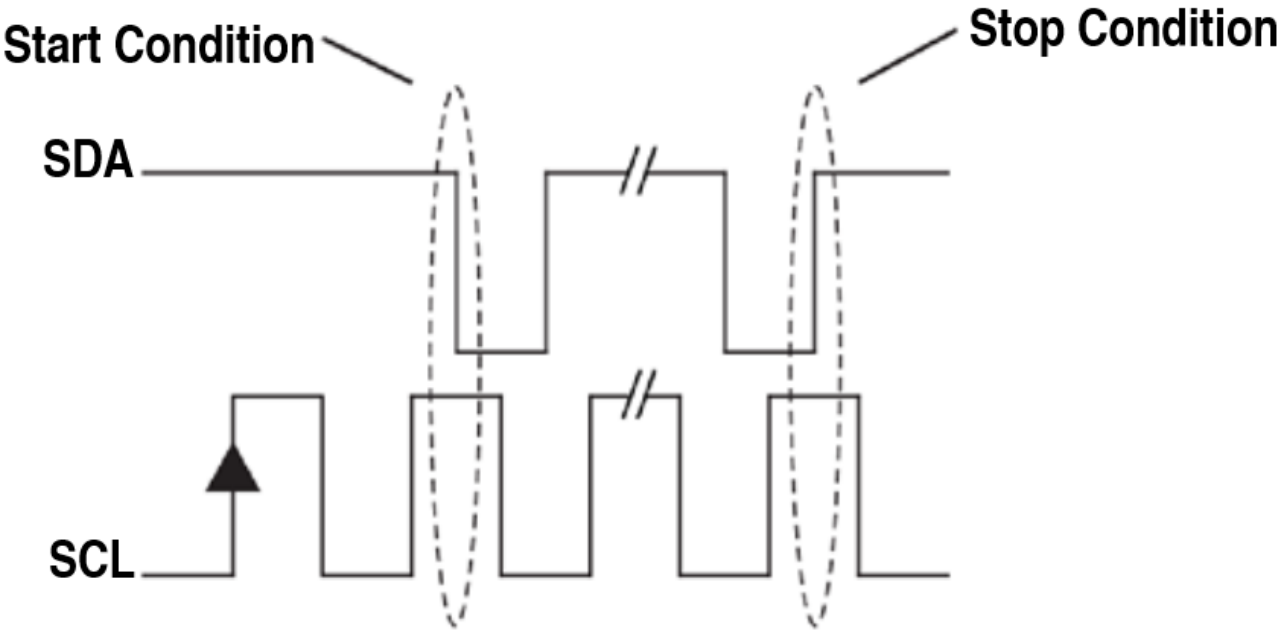


Figure 5. Start and Stop Transition Conditions

When SCL is logic-high, a Start condition is created by the SDA's **falling** edge. This initiates data transmission. Conversely, a Stop condition, which occurs at the end of a data transfer, is created by the SDA's **rising** edge when the SCL signal is a logic high. Both conditions are generated by the Master device. When the Stop command is given, all Slave devices enter an idle state, release the SDA line, and cease data transfer on the bus. In all other conditions, the SDA signal only changes state when the SCL signal is a logic low.

Following a Start command, a Slave device will respond when it recognizes the

address byte by issuing an acknowledgement bit by pulling SDA to a logic-low on the ninth CLK cycle. Until the Master issues a stop bit, the data transfer continues.

Acknowledge and Not Acknowledge Bits (ACK/NACK)

After every byte transmission, feedback is created by the receiving device using an Acknowledge or Not Acknowledge bit. Holding the SDA line low during a HIGH SCL period creates an Acknowledge bit, whereas a Not Acknowledge bit is generated when the receiver leaves the SDA line passively pulled HIGH and does not respond. This characteristic makes it clear that in response to an address byte, all Slaves with a non-matching address send a Not Acknowledge bit by not responding.

An ACK bit denotes that a byte (address or data) was transmitted and received successfully, and that the transmission can either continue to the next byte transfer or a stop condition or a repeated start can be issued (Figure 6).

The receiver can use a NACK to indicate the presence of an error somewhere in the data transmission. The NACK signals the transmitting device to terminate the transmission immediately or to make another attempt by sending a repeated start.

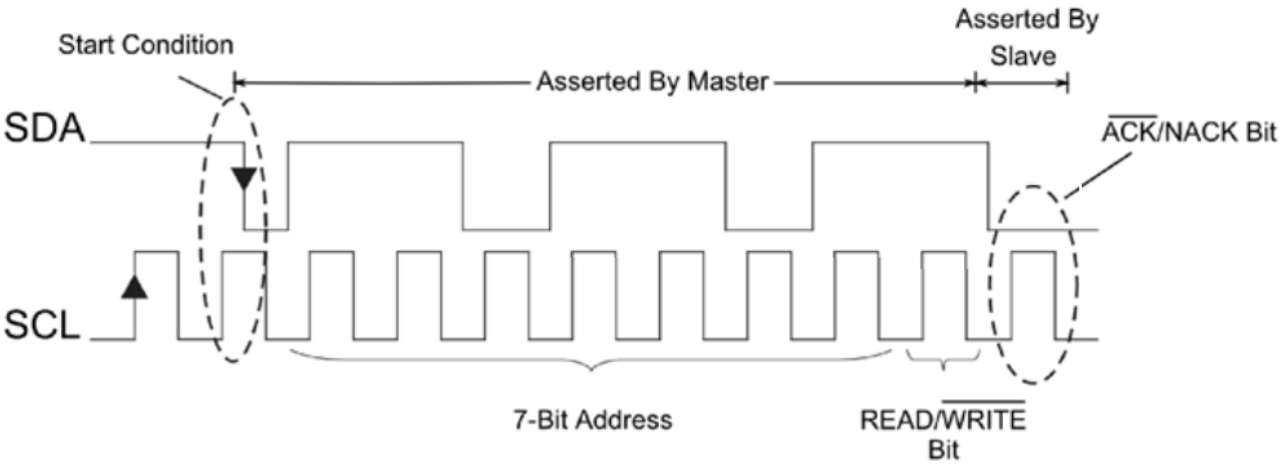


Figure 6. A Signal Diagram Showing a Start Condition, 7-bit Address of 0x6D and a Read Command. The Slave Device Responds with a (logic-low) Acknowledgment.

Data Bits

The transmission data is encoded as data bits and transmitted in an 8-bit format, MSB first. Each bit is synchronized with the SCL signal, as shown in Figure 7. The data on the SDA line must remain stable during the SCL's logic-high period. Data can only transition between logic states when the SCL signal is a logic low. The receiver reads a data bit while the SCL state is logic high. The transmitter asserts

each bit only while SCL is a logic low. There are no limits to the number of bytes in a transmission. An Acknowledge bit, generated by the recipient, must follow each byte.

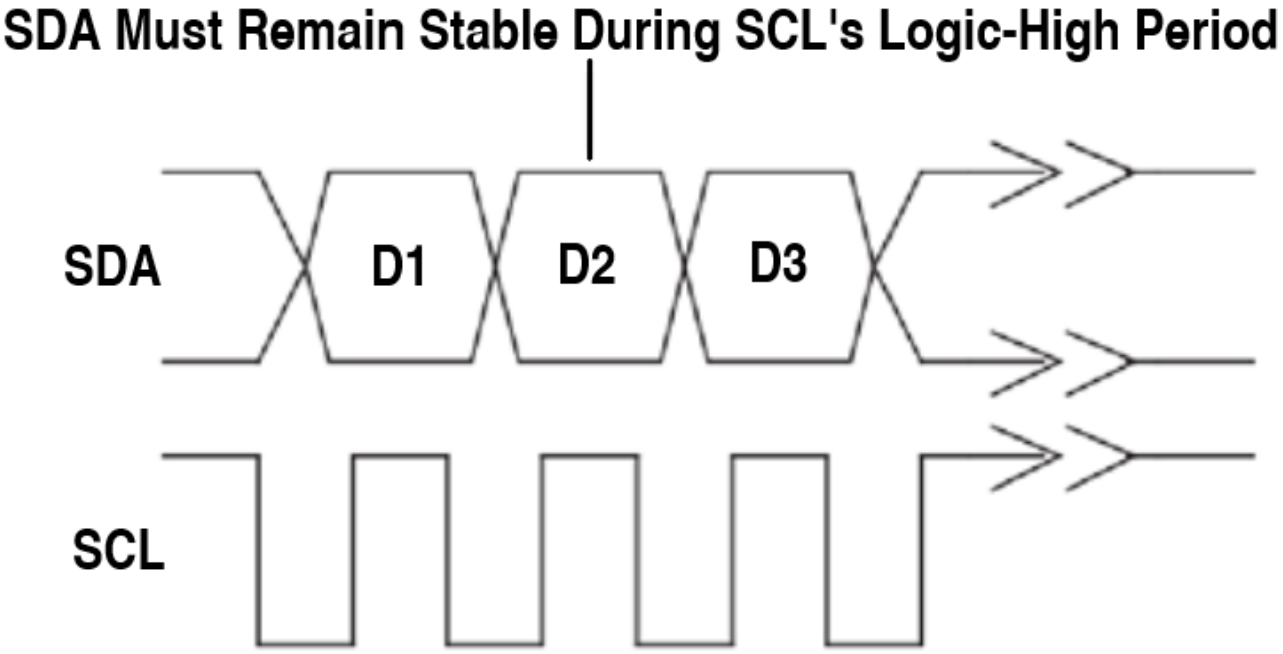


Figure 7. Bit Transition for Valid Data Bits.

Register Description (See Notes 1 and 2 below.)

Address	Bit Address	Register Name	Default Value	Description
0x30	7 – 4	Sleep time <3:0>	4'b0000	0000b: 62.5ms 0001b:125ms …. 1111b:1s[1]
	3	SCO	1'b0	1[2]
	2 - 0	Measurement CTRL <2:0>	3'b000	000b: single temperature acquisition mode 001b: single pressure acquisition mode 010b: combines a pressure acquisition followed immediately by a temperature acquisition 011b: sleep mode[3]

Note 1: Address 0x30, bit 2 – bit 0 represents collection mode.
Note 2: After sending the conversion instruction to address 0x30, interrogate address 0x20, bit 0. A logic 1 in bit 0 signifies that the conversion is completed and automatically resets to 0 after the read. A logic o in bit 0 signifies that a conversion is in progress and data is not ready to read.
[1] Only valid in sleep mode.
[2] Set to 1 as data collection begins. Automatically resets to 0 when collection ends.
[3] While sleep mode is active, a combined acquisition occurs at intervals determined by Sleep time.

Pressure Data Register Description (See Notes 1, 2, and 3 below.)

Address	Bit Address	Register Name	Default Value
0x06	7 – 0	PDATA <23:16>	0x00
0x07	7 – 0	PDATA <15:8>	0x00
0x08	7 – 0	PDATA <7:0>	0x00

Note 1: Signed two's-complement number.
Note 2: When RAW_P is a logic high, the raw data of the pressure/temperature channel is stored.
Note 3: When RAW_P is a logic low, the pressure calibration data is stored.

The ADC's digital output has 24-bit resolution. Its MSB is the sign bit, designating a positive or negative value.

Pressure Data Decimal Conversion

Given the hexadecimal values found in addresses 0x06, 0x07, and 0x08 converting them to decimal is accomplished using Equation 1.

$$\text{Decimal Value} = \text{Dec}(0x06)(2^{16}) + \text{Dec}(0x07)(2^{8}) + \text{Dec}(0x08)(1) \quad (1)$$

The values generated by Equation 1 can be **normalized** according to the following rules:
If Equation 1's result is greater than 2^{23}, then the normalized value is:
$(\text{Decimal Value} - 2^{24})/(2^{23})$
If Equation 1's result is less than or equal to 2^{23}, then the normalized value is:
$(\text{Decimal Value})/(2^{23})$

The resultant pressure value P is determined by:
$P = (P_H\text{-}P_L)/A*(\text{ADC } \textbf{normalized} \text{ value } -B)+P_L$

Where
P = Calculated pressure value
P_H = Air pressure range, upper limit: 18.86psi
P_L = Air pressure range, lower limit: 4.35psi
A = Transfer function coefficient: 0.8
B = Transfer function coefficient: 0.1

A Pressure Calculation Example

Pressure Range		Output Voltage		Transfer Function Coefficient	
P_L	P_H	Zero Count	Full-Scale Count	A	B
17.405psi	29.008psi	$0.1*V_{DD}$	$0.9*V_{DD}$	0.8	0.1

The following is assumed that the following relation applies after sensor calibration.

Correspondence Calibration	Zero Code	Full-Scale Code
Apply Pressure Value	17.405psi	29.008psi
Expected Value	0.1	0.9
Corresponding Decimal Value	2^{20}*0.1 =104858	2^{20}*0.9 = 943718

Assuming that the pressure value in 0x21946a, which normalizes to 0.2623. The temperature decimal output is 63868. The result:

Pressure Value = $\frac{(29.008-17.405)}{0.8} x(0.2623 - 0.1) + 17.405$

$= 19.759psi$

Temperature Data Register Description (See notes 4, 5, and 6 below.)

Address	Bit Address	Register Name	Default Value
0x09	7 – 0	PDATA <23:16>	0x00
0x0A	7 – 0	PDATA <15:8>	0x00

Note 4: Signed two's-complement number.
Note 5: When RAW_T is a logic high, it is undefined.
Note 3: When RAW_T is a logic low, the temperature calibration data is stored.

The ADC's digital output has 16-bit resolution. Its MSB is the sign bit, designating a positive or negative value.

Temperature Data Decimal Conversion

Given the hexadecimal values found in addresses 0x09 and 0x0A converting them to decimal is accomplished using Equation 2.

Decimal Value = Dec(0x07)(2^8) + Dec(0x08)(1) (2)

The values generated by Equation 2 can be **normalized**, which produces the actual temperature value, according to the following rules:
If Equation 2's result is greater than 2^{15}, then the normalized value is:
(Decimal Value – 2^{16})/(2^8)
If Equation 2's result is less than or equal to 2^{15}, then the **normalized** value is:
(Decimal Value)/(2^8)

Master Device Writing Data to Slave Device

A Master device addressing and writing data received by a Slave device is shown in the Figure 8 signal diagram. Initiating communication, the START bit is the first bit

sent. This is followed by the address byte. During this transmission, all Slave devices are monitoring the first seven bits of the address byte, looking to see if it matches their unique address. The Slave device that finds an address match listens for the last bit to determine if a read from, or write to, the Slave will occur. All remining Slave devices, since their addresses do not match that sent by the Master, ignore further communication, and send a NACK.

The Slave device that recognizes the address and write command responds with an ACK (acknowledge) bit. This informs the Master that the Slave device is active on the bus and waiting for further communication. The Master proceeds by sending byte-format data. The Master can write to a specific Slave device register by writing the command byte before sending the data. After a byte transfer, the Slave issues an ACK bit. When data transfer ends, the Master terminates the transfer by issuing a STOP condition (both SDA and SCL are set to a logic high).

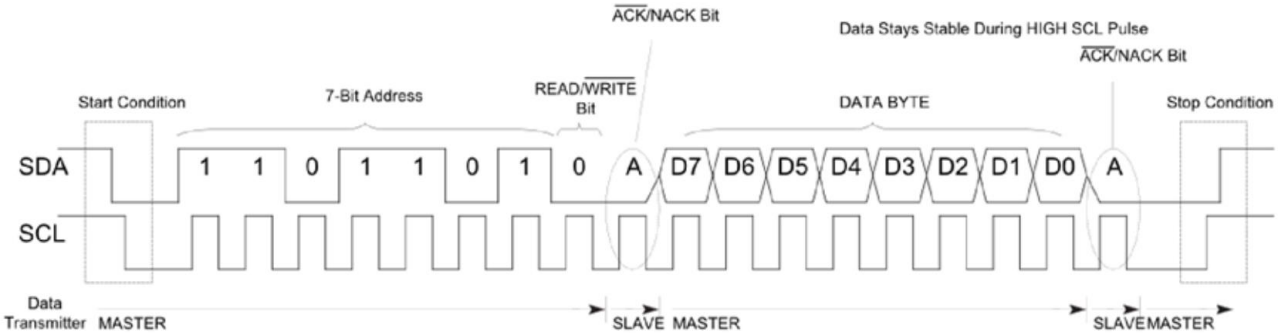


Figure 8. I²C Write Sequence Transmission

Master Device Reading Data from Slave Device

A Master device addressing and reading data sent by a Slave device is shown in the Figure 9 signal diagram. Initiating communication, the START bit is the first bit sent. This is followed by the address byte. During this transmission, all Slave devices are monitoring the first seven bits of the address byte, looking to see if it matches their unique address. The Slave device that finds an address match listens for the last bit to determine if a read from, or write to, the Slave will occur. All remining Slave devices, since their addresses do not match that sent by the Master, ignore further communication, and send a NACK.

The Slave device that recognizes the address and read command responds with an ACK (acknowledge) bit. This informs the Master that the Slave device is active on the bus, The Slave transmits byte-format data. The Master sends an ACK bit at the end of each byte. When the Master receives all necessary and requested data, it responds with a NACK bit. The Master then resumes bus control. The Master

then terminates the transfer by issuing a STOP condition (both SDA and SCL are set to a logic high).

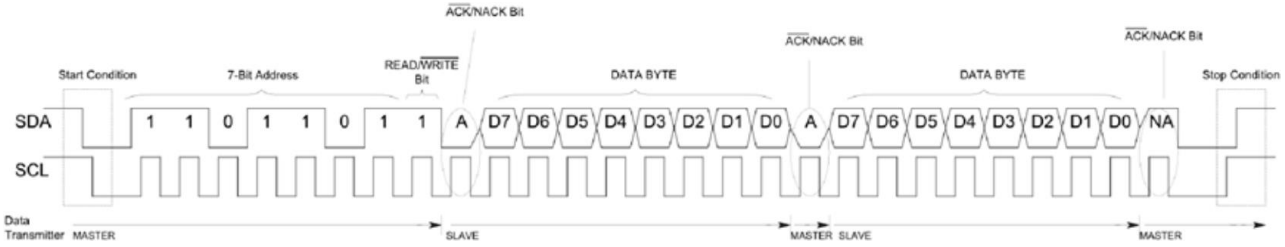


Figure 9. I²C Read Sequence Transmission

Whereas control of the SDA line is passed between the Master and the various Slaves, the SCL line is always controlled by the Master; it always clocks the data, whether going to a Slave or coming from the Slave to the Master.

SPI

The PSD0603130's SPI bus uses four signals on the CSB (active-low Chip Select), SCL (Serial Clock), SDI (Serial Data Input), and SDO (Serial Data Output) pins. The typical connections are shown in Figure 10.

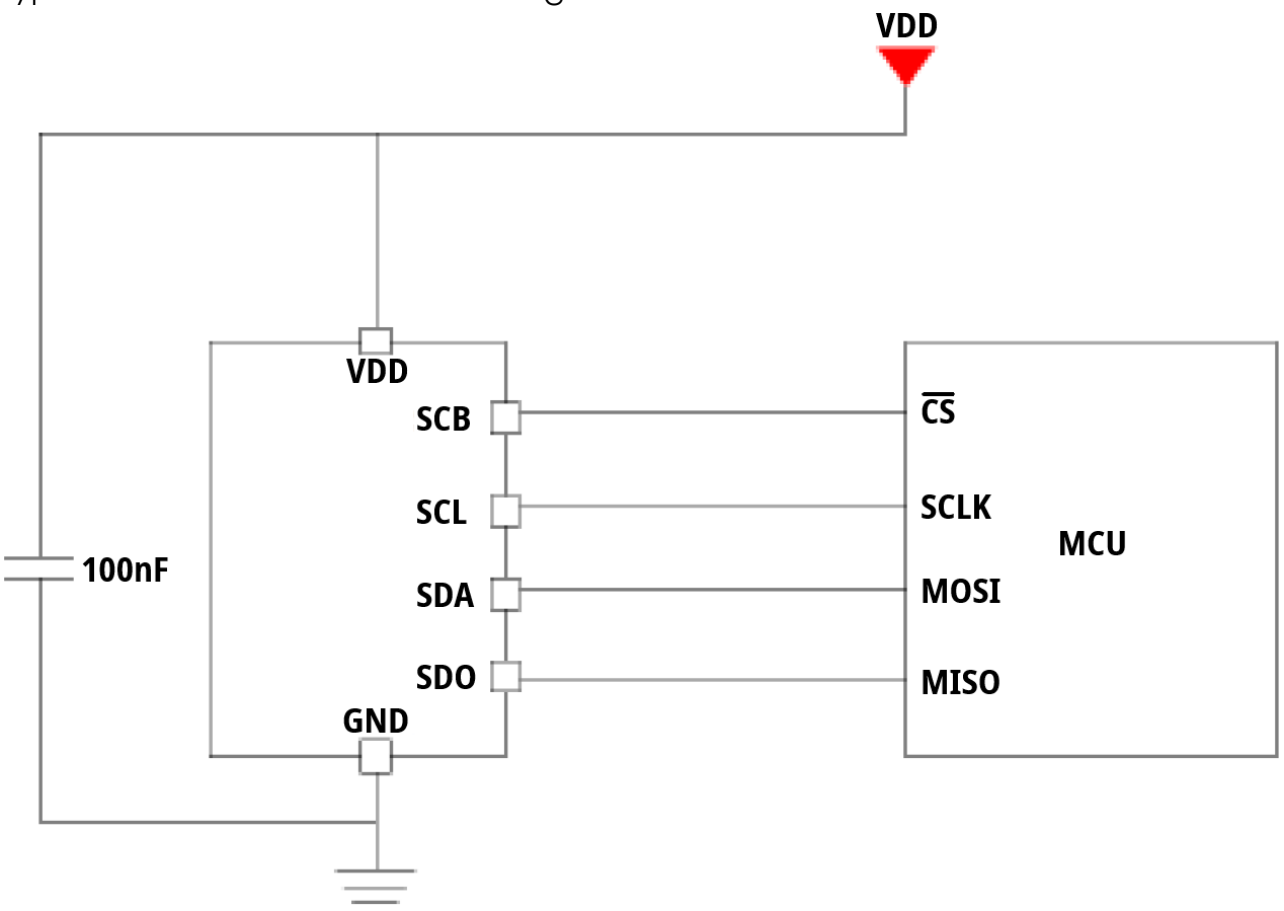


Figure 10. Typical SPI Serial Connections Diagram

SPI is a full-duplex, Master/Slave synchronous interface. Data from either the Master or Slave is synchronized to the clock signals rising or falling edge. The Master and any Slave can transmit data simultaneously. An SPI interface can be implemented as a three-wire or four-wire interface. The applications information presented here is for a four-wire interface. These four signals include:

- Clock (SPI CLK, SCLK)
- Chip Select ($\overline{CS}$)
- Master Out, Slave In (MOSI)
- Master In, Slave Out (MiSO)

The Master generates the clock signal, to which any data the is transmitted between a Master and any Slave is synchronized. Compared to I²C, SPI uses clock signals capable of much higher frequencies, 400kHz versus 10MHz, for the PSD0603130.

An SPI interface must have only one Master, but multiple Slaves. An individual Slave is selected by the Master when it asserts a logic-low on the selected Slave's $\overline{CS}$ input. Once the data transfer is completed, the Master asserts a logic-high on the Slave's $\overline{CS}$ input, disconnecting the Slave from the SPI bus. Each Slave requires a unique chip select output from the Master.

MOSI and MISO are data lines. MOSI transmits data from the Master to a selected Slave, whereas MISO transmits data from the Slave to the Master. R/$\overline{W}$

SPI Data Transmission

An SPI communication begins when the Master generates an active clock signal and asserts a logic-low on the selected Slave's $\overline{CS}$ input. As SPI is a full-duplex interface, the Master and a Slave can transmit data to each other simultaneously using the MOSI (Master) and MISO (Slave) lines. During SPI communication, data is simultaneously transmitted (serially shifted out on the MOSI/DSO line) and received (serially shifted in (sampled) on the MISO/SDI line). The serial clock's rising edge synchronizes the received data on the MISO line and its falling edge synchronizes the shifted data output on the MOSI line. The SPI interface allows the flexibility of choosing which clock edge is used for either shifting out or shifting in (sampling) data.

The Master SPI device determines the clock polarity and the clock phase based on the requirements of the Slave device. The DSP6230130 uses SPI Mode 0. In this mode, the CLK idle state is logic-low, the data is sampled on the rising CLK edge, and the data is shifted out on the falling CLK edge. A typical timing configuration

is shown in Figure 11.

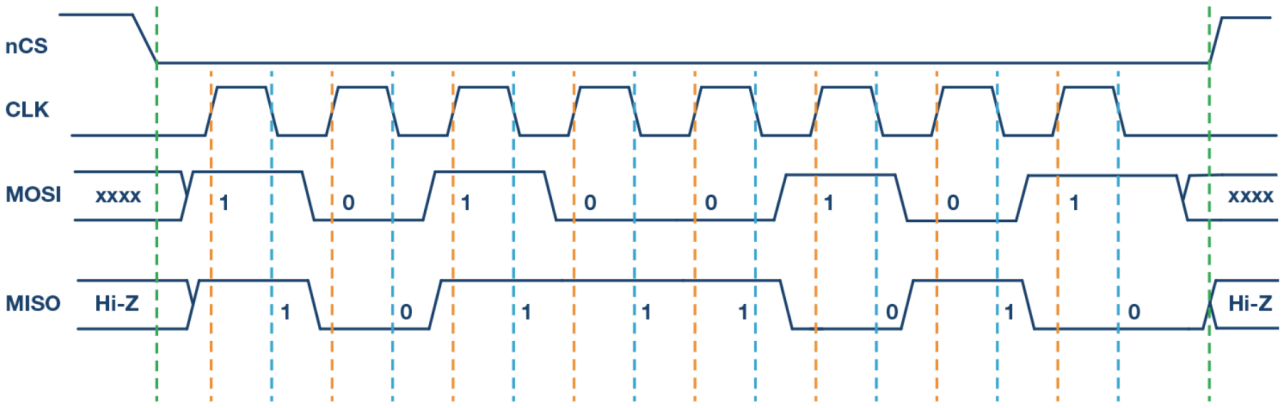


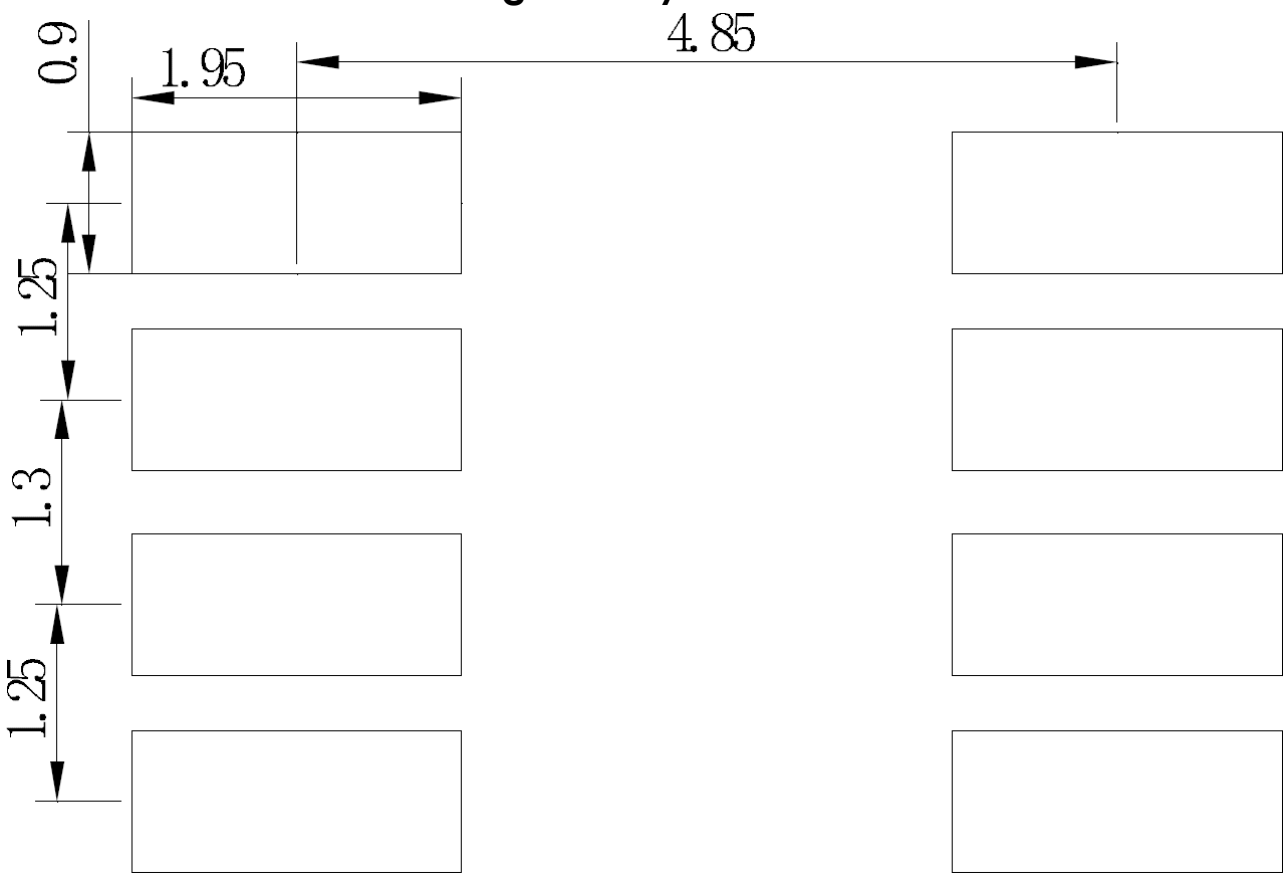
Figure 11. The PSD0603130 is Internally Configured for SPI Mode 0. The CLK's Idle State is Logic Low, Data is Sampled on the CLK's Rising Edge, and Data is Shifted on CLK's Falling Edge.

The data MSB (bit 15) on the MOSI line is the R/$\overline{W}$ bit, followed by W1 (bit 14) and W0 (bit 13). W1 and W0 are used to select any of the four functions associated with the four registers shown in Figure 12. When $\overline{CS}$ is a logic-low, the number of bytes transferred is determined by the value of W1 and W0. When set to 00, 01, or 10, $\overline{CS}$ can be set to a logic-high between byte transfers, even if the number of transfers is less than designated. Transfer resumes when $\overline{CS}$ is set to a logic-low until the specified number of byte transfers are complete. When these two bits are set to a logic-high, the number of byte transfers is unlimited while $\overline{CS}$ is a logic-low. In this last mode, $\overline{CS}$ must remain low and cannot be changed to a logic-high between bytes.

W1: W0	Function	$\overline{CS}$ Logic State
00	Send one data byte	Flexible – can return to logic-high between bytes
01	Send two data bytes	Flexible – can return to logic-high between bytes
10	Send three data bytes	Flexible – can return to logic-high between bytes
11	Send four or more data bytes	$\overline{CS}$ remains logic-low until data transfer is complete

Figure 12. Byte Transfer Count and $\overline{CS}$ Function.

Recommended PCB Landing Pad Layout and Dimensions



Assembly Recommendations

Soldering and Assembly

The PSD0603130 has a small physical structure, which means that its thermal capacity is limited. Therefore, during the reflow process use only the heat necessary to complete PCB assembly. Excess heat beyond that necessary for proper reflow may cause thermal deformation that can alter and degrade the sensor's performance characteristics. Additionally, ensure that flux or other debris is not allowed to invade the device's interior.

SMT Soldering

The reflow heat profile shown in Figure 13 is recommended.

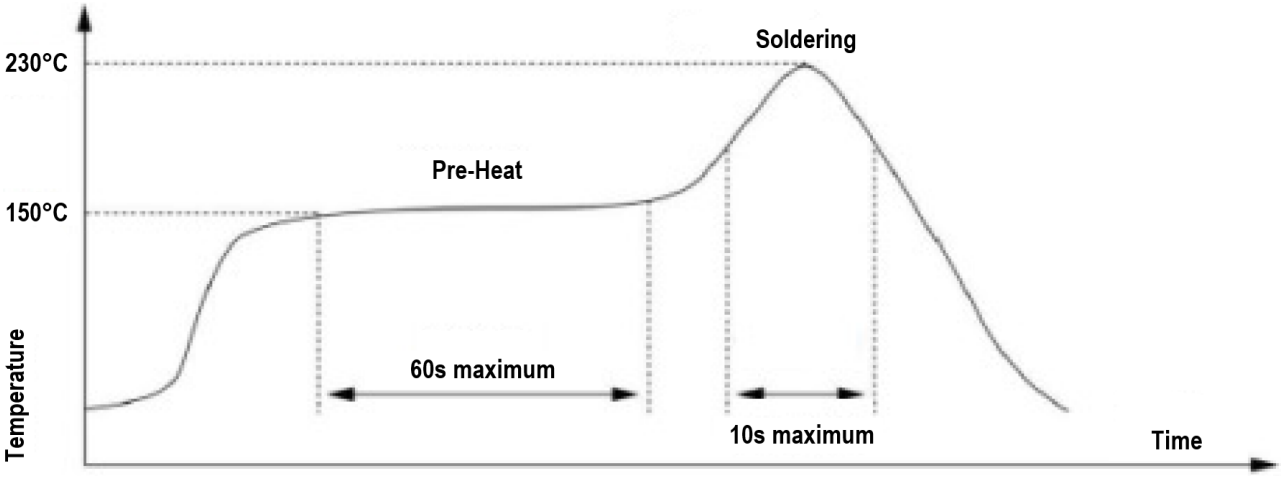


Figure 13. Recommended Solder Reflow Timing and Temperature Profile.

Cleanout

During manufacturing, the PSD0603130 is assembled in a dust-free environment. It is recommended that the PCB assembly process is also performed in a dust-free environment (Class 7, ISO14644-1 is suggested). If not possible, use a temporary cover over the sensor during assembly that prevents dust or particles entrance into the device's interior. Since post reflow cleaning increases the risk of damage to the sensor, the use of "no-cleaning" solder paste is recommended.

Sensor Port

The sensor is located internally below the device's port. Any foreign object that enters the port can cause damage, rendering the device damaged and leading to errant data or completely inoperable. Therefore, using an acoustically transparent protective membrane is encouraged.

Environment

To avoid the sensitivity and output value changes, avoid exposing the sensor to light sources.

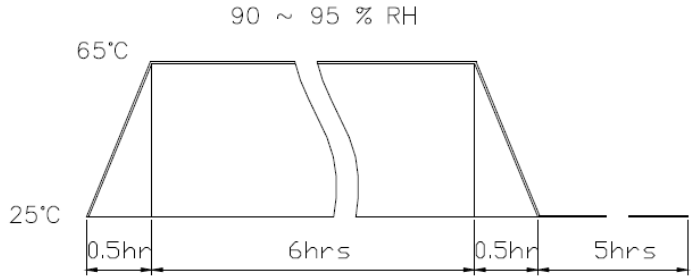
Pressure Range

Ensure that the range of pressure that will be measured is within the range of the sensor. Pressures outside this range can damage the sensor.

ESD Protection

Ensure that when stored prior to assembly onto a PCB that the PSD0603130 is stored in an ESD protective container. Please practice proper ESD protocols to prevent ESD damage while handling the device.

Reliability Testing

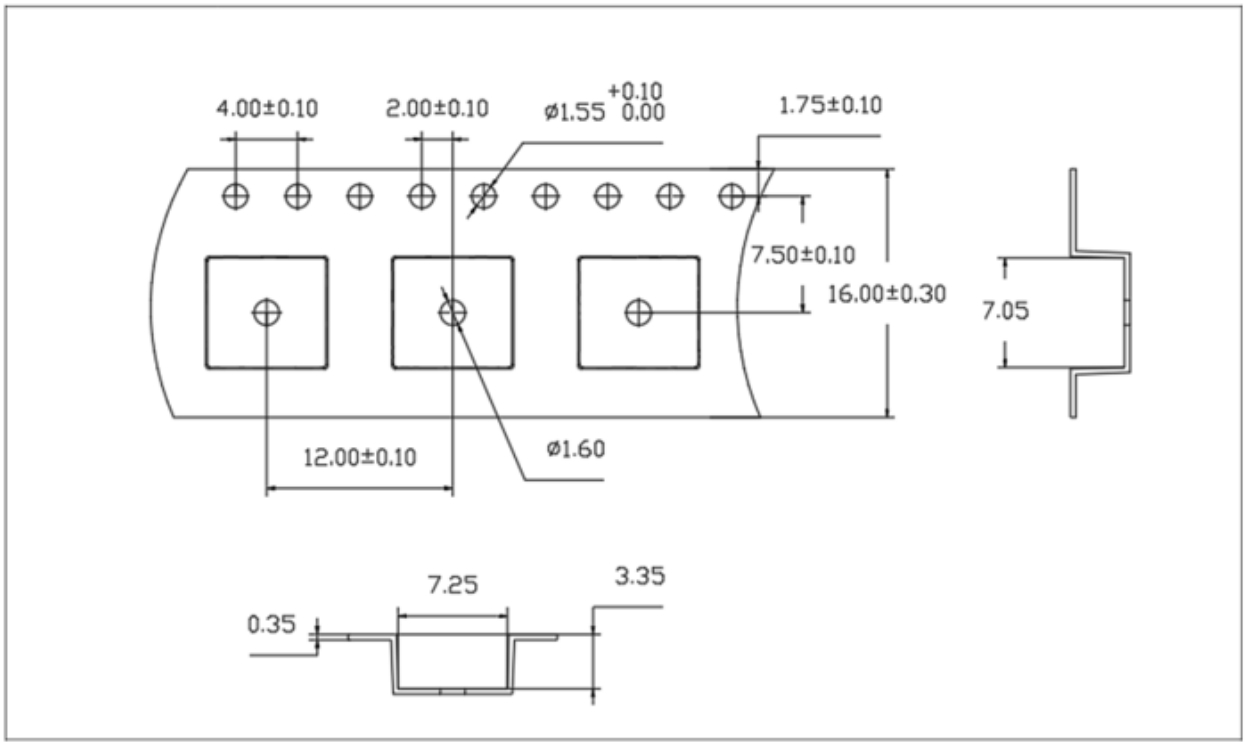
Type of Test	Test Specifications
High Temperature Test	96 hours at 70±3°C
Low Temperature Test	96 hours at -30±3°C
Humidity Test	96 hours at 30±3°C with relative humidity at 92~95%
Temperature Cycle Testing	Run for 5 cycles with each cycle consisting of: 
Vibration Test	Frequency: 10~55~10Hz Oct/min Amplitude: 1.5mm Duration: 2 hours each of 3 perpendicular directions
Drop Test	Drop the speaker contained in normal box onto the surface of 40mm thick board 10 times from the height of 75cm.
Load Test	Must perform normal with program White-Noise source at Rated Power for 96 Hours

After each test let rest for 6 hours in standard room temperature, the part shall be within ±3dB.

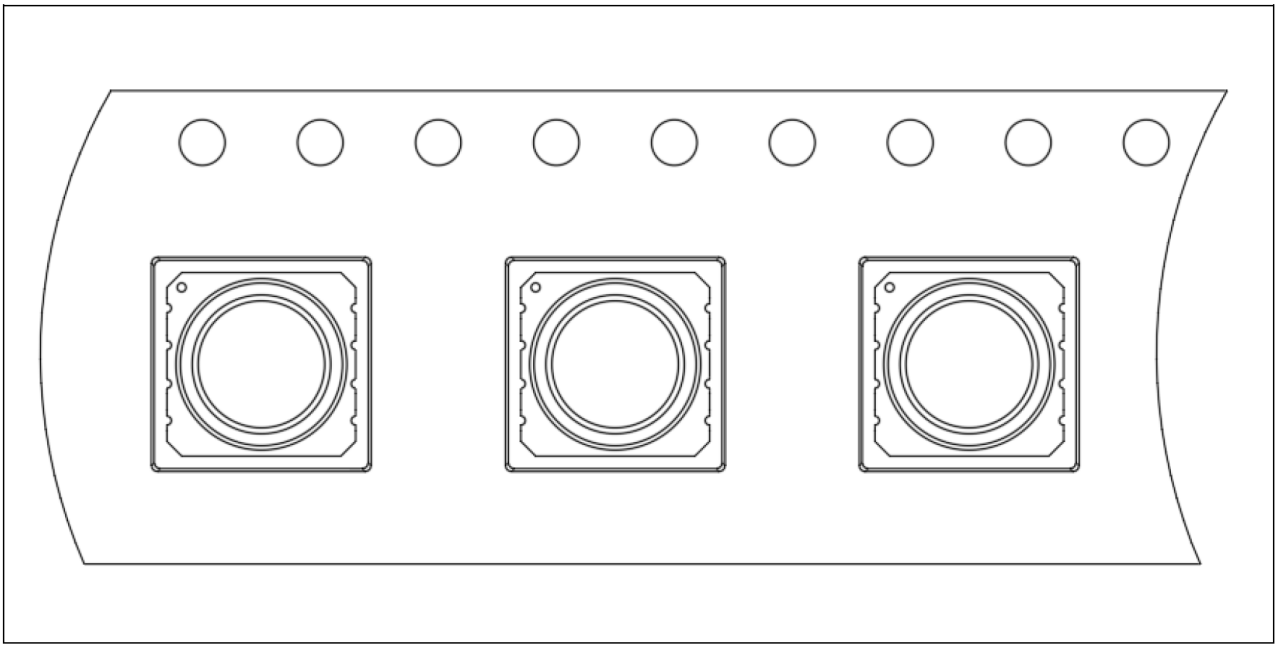
Packaging

Reel Specifications

1 Reel = 1,500 pcs
1 Box = 4Reels =6,000pcscen



Device Orientation



Specifications Revisions

Revision	Description	Date	Approval
A	Datasheet from Engineering	10/30/2023	KH
B	Various edits: pages 2, 4, 10, and 11	12/04/2023	KH
C	Update in the specification table, page 2.	12/13/2023	KH
D	Update to the suggested landing pattern, page 16.	02/27/2024	KH

Note:

1. Unless otherwise specified:
    A. All dimensions are in millimeters.
    B. Default tolerances are ±0.5mm and angles are ±3°.
2. Specifications subject to change or withdrawal without notice.